Remarks

These remarks are in response to the Office Action of November 2, 2005, for which a one-month extension is hereby requested. The Office objected to claim 91, which has now been rewritten in independent form as written below. The Office Action also rejected all of the pending claims, claims 1-7, 9-20, 22-39, 52-58, 61-65, 76, 77, and 91-98, under 35 U.S.C. 102(b) as being disclosed by Jiang et al., "Key Hot-Carrier Degradation Model Calibration and Verification Issues for Accurate AC Circuit-Level Reliability Simulation", IEEE 1997, pp. 300. As discussed below, it is respectfully submitted that these rejections are in error.

The Jiang et al. reference is concerned with the modeling of hot-carrier degradation effects, as is the present application; however, Jiang concerns are the calibration and evaluation of such models as they are found in the prior art. The pending claims of the present application are drawn to a number of aspects of the present invention that are not believed to be found in the prior art in general and that are not found in Jiang in particular. Several of these aspects and the claims that present them are discussed below the various headings.

Claims 1-7

Claim 1 is drawn to an aspect of the present invention that allows for simulating for multiple stress time values in a single run, as is described, for example, beginning on line 7 of page 8 of the present application. It is respectfully submitted that such a method is neither taught nor suggested by Jiang. Although believed allowable in its original form, claim 1 has been amended to make it even more explicit that this simulation for multiple stress time values is performed as part of a *single* simulation run.

More specifically, claim 1 has as its second step:

> supplying a plurality of circuit stress time values;

and ends with

> determining the degraded operation of the circuit by *simulating in a single run the operation of the circuit* with the specified components using their respective aging model information and respective relative component degradation parameter *at the plurality of supplied circuit stress time values*.

The emphasis has been added and the underlined elements have been added in the current amendment. For these limitations, the Office Action variously cites Jiang at page 300, the Introduction; page 300, right column, lines 10-11; and page 305, right column, second paragraph. It is respectfully submitted that neither in these locations nor elsewhere does Jiang disclose simulating multiple stress time values in a single run.

Concerning these three portions of Jiang, cited both with respect to claim 1 and elsewhere in the Office Action, the Introduction is about calibration and verification issues to make sure that when the verification is done, it is more accurate. These are the subjects with which the Jinag reference is concerned. The Introduction is not about what actually goes on during the simulation and more or less assumes the prior art to actually perform the simulation---a more accurately calibrated prior art, but still the prior art. In particular, it neither teaches nor suggests including multiple stress time values within a single run with a circuit simulator.

As for page 300, right column, lines 10-11, this just states that parameter extraction was performed. Such a step is needed to supply parameters to the (in Jiang) SPICE simulator so that the simulation can be performed, or perhaps to extract parameters values after they have degraded, but this is not part of running an actual simulation.

Finally, concerning page 305, right column, second paragraph, this paragraph just refers to a specific "time period", namely when switching occurs in a static CMOS digital circuit, and notes that such periods are of particular importance in *calibrating* models; it does not refer to stress time values at which the degraded operation of the circuit is determined. Consequently, it also neither teaches nor suggests including multiple stress time values within a single run with a circuit simulator.

Therefore, for any of these reasons, it is respectfully submitted that a rejection of claim 1, along with its dependent claims (2-7, 9-20, 22-39, 52-58, 61-65, 76, 77, and 93-98), under 35 U.S.C. 102(b) as being anticipated by Jiang is in error and should be withdrawn.

Concerning claim 4, this includes the further limitation of "wherein the simulating is performed using a timing simulation type circuit simulator", for which the Office Action cites Jiang at page 300, Abstract and "Summary of existing Model"; however, this only refers to a SPICE type simulator (examples being as HSPICE or Spectre) and has no reference to a timing simulation type of simulator (such as Starsim or Timemill). In fact, the main subject of the Jiang

paper specifically related to SPICE simulators and their calibration and accuracy. Consequently, claim 4 is believed further allowable on this basis.

As for claim 5, the Office Action appears to be making improper assumptions as to what is "inherent" without supplying a substantiating reference. Aging model could well be supplied from other sources besides electrical test data, a limitation for which the Office Action provides no citation.

Concerning claim 6, this contains the limitation of "said simulating the behavior of the fresh circuit determines the waveforms at the nodes to which the selected ones of the components are connected relative to an input waveform", for which the Office Action cites Jiang at page 304, left column, last paragraph: however, this paragraph discusses the operation of the degraded circuit, not "simulating the behavior of the fresh circuit"; and it has no disclosure at all of waveforms, whether input waveforms or waveforms at component nodes.

Concerning claim 7, the Office Action states "specification pg. 8, last two sentence disclose the speed or delay of current drain; thus results are compared to benchmark: pg. 300, introduction last 9 lines with figure 11 pg. 305". This is respectively submitted to be incorrect or improper on several grounds. First, what the specification says at the referenced location is that examples of important degradation characteristics of a digital block could be "driving capability of I_{ds} **or** the circuits delay **or** speed", where (as indicated by the added emphasis), these are alternatives: it does not state "the speed or delay ***of*** current drain" [emphasis added], as stated in the Office Action. Second, although Jiang does refer to "benchmarks", it does not, at least in the cited locations, disclose "the circuit's speed at the supplied circuit age parameters." Finally, although the cited locations may mention drain current degradation, they do not appear to disclose "circuit speed", which, contrary to the Office Action's misreading of the present application mentioned earlier in this paragraph, are not the same thing.

Claims 93 and 9-20

Claim 93 depends upon claim 1 and is believed allowable on this basis alone. Claim 93 is further drawn to an aspect of the present invention allowing different performance criteria to be applied to different circuit blocks. This is described in the paragraph beginning on page 8 at line 20. In particular, claim 93 includes the step of

supplying an independent performance criterion for each set of said plurality of distinct sets of components;

It is respectfully submitted that such a step is neither taught nor suggested by Jiang–in fact, the Office Action provides no reference to Jiang for this limitation. For other portions of the claim, found in the following "wherein" clauses, the Office Action refers generally to Jiang's Introduction; however, as has been noted the Introduction is concerned with calibration and verification issues and has no disclosure of "supplying an independent performance criterion ..." as is found in claim 93. Consequently, a rejection of claim 93, along with its dependent claims 9-20, under 35 U.S.C. 102(b) as being anticipated by Jiang is believed to be further in error on this basis.

Concerning dependent claims 9-20, first it is noted that in the rejection of claims 9, 10, and 20, the Office Action states "specification, pg 6, line 3 defines functional blocks 'analog to digital sector': this is incorrect and explicitly contrary to the limitations of some of the claims for which this statement is made. What the application actually says is "blocks, such as an analog sector and a digital sector"; that is, *examples*, not a definition, of such blocks could be an analog sector or a digital sector, *not* an "analog to digital" sector.

As to the specifics of claims 9 and 10, the Office Action cites the last 9 sentences on the left column of page 300 of Jiang. However, this provides no disclosure of segregating circuit components based on either of "different functional blocks" (as in claim 9) or of "analog block and ... a digital block" (as in claim 10); in particular, Jiang does not specify "independent performance criteri[a]" based on such distinctions.

Concerning claim 11, this includes transconductance as a performance criteria, something which is not believed to be found in Jiang and for which the Office Action provides no reference. (The Office Action does state "design choice, see In re Stevens"; however, it would appear that, at the least, the cited reference would need to provide the needed elements from which the choice is to be made.)

As to the specifics of claim 12, the Office Action cites the "AC Degradation Model Validation section on page 300 of Jiang. However, this provides no disclosure of segregating circuit components based on "device type"; rather, the comparison is for different *technologies*, as discussed in Jiang's "EXPERIMENTAL DETAILS" on page 300. Basically, these are for the same device types, but have differing dimensions.

Concerning claims 14, 16, and 17, these specify that a performance criterion is "leakage current" (claims 14 and 17) and that "a second of said device types is a bipolar junction transistor" (claims 16 and 17). For the first of these, the Office Action states "reverse bias of a transistor and thus inherent", without any reference to Jiang. As far as can be determined, Jiang has no disclosure of using leakage current as performance criterion (or, apparently, otherwise; further, the Office Action is making improper assumption about what is inherent without providing a substantiating reference. As for bipolar junction transistors, the Office Action provides no reference to Jiang and this also appears not to be disclosed in Jiang, either generally or, as found in the claim, as a criterion for segregating components according to device type.

Concerning claim 18, the Office Action again cites the "AC Degradation Model Validation section on page 300 of Jiang. However, this provides no disclosure of "different models for simulating the same device type." Rather, a comparison is discussed for different *technologies*, as discussed in Jiang's "EXPERIMENTAL DETAILS" on page 300. Basically, these are for the same device types, but have differing dimensions, and there is no disclosure of using "different models for simulating the same device type."

Claims 94 and 22-39

Claim 94 depends upon claim 1 and is believed allowable on this basis alone. It is believed further allowable as it also drawn to the aspect of the present invention presented whereby the depredation level of selected components can be specified, as opposed to determining the level of degradation for other elements. This is described, for example, beginning on page 9, line 20, of the present application as part of optional step 103 in Figure 5. In particular, claim 94 includes the additional step of:

> specifying the degradation level of a second set of selected components of the circuit, wherein the elements of the first set and the second set of components are distinct,

where the degraded operation of the circuit then uses these specified values for the selected set of components, while the other set of components again uses the determined level of degradation. For this limitation, the Office Action refers to page 300, Introduction, of Jiang. This is respectfully submitted to be in error. As before, Jiang's Introduction is about calibration and verification issues to make the prior art more accurate; it is not about what actually goes on during the simulation and more or less assumes the prior art. And in particular, it neither teaches

nor suggests performing a simulation to determine the degraded operation of a circuit with a subset of the components having their degradation level pre-specified. Consequently, a rejection of claim 94, along with its dependent claims 22-39, under 35 U.S.C. 102(b) as being anticipated by Jiang is believed to be further in error on this basis.

Dependent claims 22-36 are drawn to various examples of what the "first set" and "second set" of components may be, and to various examples of how the degradation level may be specified. First it is again noted that in the rejection of claims 22, 23, and elsewhere, the Office Action states "specification, pg 6, line 3 defines functional blocks 'analog to digital sector': this is incorrect and explicitly contrary to the limitations of some of the claims for which this statement is made. What the application actually says is "blocks, such as an analog sector and a digital sector"; that is, *examples*, not a definition, of such blocks could be an analog sector or a digital sector, *not* an "analog to digital" sector.

As to the various specifics of claim 22-36, for many of these the Office Action just generally refers to Jiang's Introduction; however, reference to many of these (e.g., transconductance, an analog block, leakage current, bipolar junction transistors, the use of differing models for devices of the same type, and so on) is not found there. Consequently, it is believed that these dependent claims are generally further allowable on this basis.

Concerning claims 37-39, these give specific examples of ways of specifying the level of degradation. In claim 37, "the degradation level of the second set of selected components is specified as a relative component degradation parameter with respect to the component degradation parameter of the first set of components", for which the Office Action also cites Jiang's Introduction. It is respectively submitted that the use of such a relative scale of degradation is not found in Jiang's Introduction or, as far as can be determined, elsewhere in Jiang.

In claim 38, "the degradation level of the second set of selected components is expressed in terms of age", for which the Office Action cites page 303, right column, first paragraph of Jiang; however, this paragraph discusses the importance of using the correct model parameters for the simulator. This is no disclosure of a "degradation level ... expressed in terms of age."

In claim 39, "the degradation level of the second set of selected components is expressed in terms of lifetime", for which the Office Action cites Jiang at page 305, right column, second

paragraph, and page 303, right column, first paragraph. As for page 305, right column, second paragraph, this paragraph just refers to a specific "time period", namely when switching occurs in a static CMOS digital circuit, and notes that such periods are of particular importance in *calibrating* models. As for page 303, right column, first paragraph, this does mention "lifetime", but not as a parameter in which to express a degradation level. Consequently, claims 37-39 are believed further allowable on this basis.

Claims 95, 96 and 52-58

Claim 95 depends upon claim 1 and is again believed allowable on this basis alone. Claim 95 is further drawn to an aspect of the present invention where multiple current sources are added to represent different degradation mechanisms, as shown in Figure 6 of the present application and described beginning on page 13, line 4, with more detail given starting in the paragraph beginning on line 17 of that page. In particular, claim 95 includes the steps of:

> revising the netlist, wherein ***each*** *of said selected components is replaced by a non-aged version of the selected component and a* ***plurality of independent current sources*** *corresponding to different mechanisms connected between the terminals of the non-aged version*, wherein the magnitude of the current relative to a circuit stress time in each of the current sources of a component is determined from the aging model information of the component and a ***distinct*** *mechanism degradation parameter* derived from the component degradation parameter; and
>
> wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist at the supplied circuit stress time values.

The emphases have been added to highlight those elements that particularly distinguish this claim. For the "plurality of independent current sources", the Office Action refers to page 302, right column, "Evaluating Degradation Model Precision" section, of Jiang: however, as its title indicates, this section is about evaluating the precision of standard prior art models and has no discussion of adding current sources between the terminals of a device. Specifically, it neither teaches nor suggests replacing "selected components ... by a non-aged version of the selected component and a ***plurality of independent current sources*** *corresponding to different mechanisms* connected between the terminals of the non-aged version, wherein the magnitude of the current relative to a circuit stress time in each of the current sources of a component is determined from the aging model information of the component and a ***distinct*** *mechanism degradation parameter* derived from the component degradation parameter" [emphases added].

(For the other elements of the claim, the Office Action refers to Jiang's Introduction; page 300, right column, lines 10-11; and page 305, right column, second paragraph, which, as discussed in various places above, are not believed to be relevant.)

Consequently, a rejection of claim 95, along with its dependent claims 96 and 52-58, under 35 U.S.C. 102(b) as being anticipated by Jiang is believed to be further in error on this basis.

Concerning claim 96, this further incorporates an aspect of the present invention allowing for device models to be updated. This aspect is discussed below with respect to claim 97 and the Examiner is referred to the first paragraph under the next heading. Claim 96 is further believed allowable on this basis.

As for claim 54, the Office Action refers to "simulating drain current: pg.303, right column" of Jiang. Jiang's Figure 7 and its discussion are not related to drain-source current, but are instead about various current-voltage curves and optimizing extraction. There is no discussion of a "plurality of independent current sources ... connected between the source and drain terminals of the non-aged version", as found in the claim.

Concerning claim 55, this claim further includes "determining the magnitude of the respective current in each of the independent current sources", where said determining includes "*supplying a physical model of the current magnitude*" [emphasis added]. As far as can be determined, Jiang has no disclosure of such supplying of physical models for current sources; further, the Office Action supplies no corresponding citation for this element. Consequently, claim 55 is further believed allowable on this basis.

Concerning claims 56 and 57, this includes the limitation that the degradation level of selected components is expressed in terms of lifetime and age, respectively. As discussed above with respect to claims 38 and 39, such limitations are not disclosed generally at the cited location in Jiang and, in particular, are not disclosed in the context in which they are found in these claims.

Claim 58 includes that the revising of the netlist is embedded in the circuit simulator. The Office Action refers to Jiang's Abstract and "Summary of existing models"; however, Jiang only discloses a SPICE simulator. This is a consequently a reference to a prior art SPICE simulator, which has no such embedding of netlist revisions, and where any revisions to the net

would need to be supplied from external to the netlist and a new simulation started over again from the beginning. Thus, claim 65 is believed further allowable on this basis.

Claims 97 and 61-65

Claim 97 depends upon claim 1 and is again believed allowable on this basis alone. Claim 97 is further drawn to an aspect of the present invention allowing for device models to be updated, as described, for example, beginning on page 15, line 18, of the present application, and is believed further allowable on this basis. In particular, the simulating of claim 97 "includes incorporating the aging of the selected components by updating the models of said circuit simulator". The Office Action cites Jiang's "pg.300, abstract and 'Summary of existing models" for this; however, neither in these locations nor, it appears, elsewhere does Jiang disclose updating the circuit simulator's models. In particular, it does not "incorporating the aging of the selected components" by such an updating. Consequently, a rejection of claim 97, along with its dependent claims 61-65, under 35 U.S.C. 102(b) as being anticipated by Jiang is believed to be further in error on this basis.

Concerning claims 61-63, these respectively include the limitation that "incorporating the aging of the selected components comprises including the time dependence of the drain to source current", "the substrate current", and "the gate current", respectively. With respect to the "time dependence", the Office Action again references page 305, right column, second paragraph of Jiang. As already discussed, with respect to claim 1 for example, this paragraph just refers to a specific "time period", namely when switching occurs in a static CMOS digital circuit, and notes that such periods are of particular importance in *calibrating* models. It does not disclose including the time dependence of any of these currents into the process of updating device models during a simulation. As for incorporating the time dependence of the specific currents recited in these claims, the Office Action only provides a reference for the source-drain current of claim 61, with none given for that of claim 62 or 63. In the right column of Jiang's page 303 the Office Action may discuss variations in the source-drain and substrate currents, but there is no disclosure of incorporating any time dependence into the simulation as is stated in these claims. Further, there appears to be no mention of the gate current (claim 63) in Jiang at all. Thus, claims 61-63 are believed further allowable on this basis.

As for claim 64, this further includes the sub-aspect of "gradual aging", described in the paragraphs beginning on page 15, line 7, of the present application. Claim 64 includes determining an "intermediate component degradation parameter" on selected components by simulating the fresh behavior of the circuit, for which the Office Action cites Jiang's Introduction. However, as discussed above, this Introduction just recites various calibration and verification issues and there is no discussion of determining "intermediate component degradation parameters". (As elsewhere, if the Office Action could be more specific as to exactly which part of the Introduction it intends to refer, the specifics could be better addressed.) Claim 64 also includes "an intermediate stress time value", for which the Office Action refers to Jiang at page 300, right column, lines 10-11, and page 305, right column, second paragraph. As already discussed, the first of these citations is for a parameter extraction that is performed prior to the simulation is even done and the second is noting periods are of particular importance in *calibrating* models; neither discloses the introduction of using "an intermediate stress time value" during the simulation of a circuit as is found in claim 64. Thus, claim 64 is believed further allowable on this basis.

Claim 65 includes that the updating of models is embedded in the circuit simulator, similar to the aspect discussed above with respect to claim 58 for revising the netlist. The Office Action again refers to Jiang's Abstract and "Summary of existing models"; however, Jiang only discloses a SPICE simulator, which has no such embedding of updating models. Thus, claim 65 is believed further allowable on this basis.

Claims 98, 76, and 77

Claim 98 depends upon claim 1 and is again believed allowable on this basis alone. It is believed further allowable as it also is drawn to the "quantizing" aspect of the present invention presented, for example, beginning on page 14, line 9, of the present application. In particular, claim 98 includes the step of

> quantizing each of said relative degradation levels to one of a plurality of discrete values;

and then using the quantized relative degradation levels at the supplied circuit stress time values. (Claim 98 has been amended for consistency with underlying claim 1.) The Office Action again cites Jiang's Introduction for these steps; however, neither in the Introduction nor, as far as can

be determined, elsewhere does Jiang teach or even disclose such quantizing of relative degradation levels. Consequently, a rejection of claim 98, along with its dependent claims 76 and 77, under 35 U.S.C. 102(b) as being anticipated by Jiang is believed to be further in error on this basis.

Claim 76 further introduces revising the netlist, as discussed above with respect to claim 95, and thus believed further allowable on this basis.

Claim 77 includes that the quantization is embedded in the circuit simulator, similar to the aspect discussed above with respect to claim 58 for revising the netlist. The Office Action again refers to Jiang's Abstract and "Summary of existing models"; however, Jiang only discloses a SPICE simulator, which has no such embedding. Thus, claim 77 is believed further allowable on this basis.

Claims 91, 92, and new claims 99-104

The Office Action objected to claim 91 as being an apparatus dependent claim linked to method claims. Claim 91 formerly depended upon claims 1 and 93-98. Claim 91 has now been rewritten in independent form by incorporating the limitations of claim 1 in order to overcome this objection. New claims 99-104 depend upon the amended claim 91 and further incorporate the limitations of claim 93-98. Consequently, each of claims 91 and 99-104 is believed allowable for the reasons given above for claims 1 and 93-98, respectively.

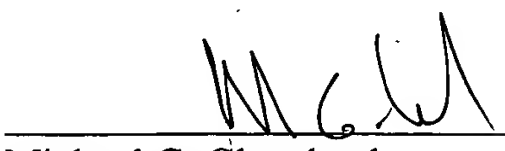
Similarly, claim 92 depends on claims 1 and 93-98 and is similarly believed to be allowable. Additionally, a rejection of this claim under 35 U.S.C. 102(b) as being disclosed by Jiang is not believed well founded as it appears that Jiang does not disclose, and the Office Action provides no citation of such in Jiang, "causing the transmission to a client device a program of instructions, thereby enabling the client device to perform, by means of such program, the process" of claims 1 and 93-98.

Conclusion

For the reasons given above, it is believed that the pending claims are allowable. Reconsideration of claims 1-7, 9-20, 22-39, 52-58, 61-65, 76, 77, 91-98, and consideration of

new claims 99-104, is respectfully requested and an early indication of their allowability is earnestly solicited.

Respectfully submitted,



2.28.06

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